JinWoo Lee

Atlanta, GA | 253-249-9658 | jlee4522@gatech.edu | International Student |linkedin.com/in/jinwoo-lee-283b59303

Education

Georgia Institute of Technology | Atlanta, GA
Bachelor of Science in Electrical Engineering — May 2028

Arizona State University | Tempe, AZ — August 2025 – December 2025
Transfer with 17 Credit Hours, GPA 4.3/4.3

Green River College | Auburn, WA — June 2025
Associate of Science in Computer and Electrical Engineering
Highest Honors, Mathematics Division Award, Foundation Scholarships
GPA 4.0/4.0

Experience

Steven Black| Auburn, WA — October 2024 – June 2025
Math Grader

- Grade weekly problem sets (5 problems) for three class sections (~60 students) in multivariable calculus and integral calculus, while communicating regularly with the instructor to ensure consistent grading policies and evaluation standards.

Adrienne Palmer | Auburn, WA — September 2024 – June 2025
Math Tutor

- Tutored undergraduate students in calculus, linear algebra, differential equations and engineering physics, 15 hours a week.
- Explained problem-solving strategies and core concepts to support students' conceptual understanding.

Projects & Activities

Digital Tram Control System Design | ASU Digital Design Project — December 2025
Designed a digital tram control system using sequential logic to meet specified operational constraints.

- Optimized a 6-state system, achieving a compact implementation with only 3 D flip-flops, 5 AND, 3 OR, and 2 NOT gates.
- Verified functionality through digital simulation and systematic testing; achieved full score on the project.

Solar Panel Monitoring System | ASU Circuit laboratory Project — August 2025 – December 2025
Built a microcontroller-based measurement system to monitor solar panel output characteristics.

- Designed an op-amp-based analog front-end for a solar panel with voltage-divider scaling to map output to the 0-5V ADC range.
- Evaluated system performance through experimental testing and documented results in technical reports.

Band-Pass Filter Design and Analysis | Engineering Physics laboratory Project — November 2024 – December 2024
Designed a passive band-pass filter to analyze physical circuit limitation through error analysis.

- Collected frequency-response data in Logger Pro and extracted 3dB cutoff frequencies to compute experimental bandwidth.
- Simulated frequency response and transfer characteristics using PSpice (OrCAD) as a validation check.
- Identified component tolerances as the primary source of percent error by comparing theoretical and measured frequencies.

Electronic Engineer Written Exam | Seoul, Korea — October 2022
Passed the national-level Electronic Engineer written exam administered by the Human Resources Development Service of Korea.

- Covered carrier transport, p-n junction behavior, BJT/FET characteristics, electromagnetics, and circuit theory.
- Reinforced understanding of circuit simulation and frequency-domain analysis using PSpice (OrCAD).

Relevant Coursework

Circuits Theory: Circuit Analysis, frequency-domain analysis, Thevenin-Norton Theorem, Op-Amps, passive filters, Bode plots
Digital Design Fundamentals: Karnaugh map, Boolean algebra, combinational and sequential logic, state-based system behavior.

Skills

Programming / HDL & Hardware: C, C++, MATLAB, Verilog, Arduino microcontroller, oscilloscope
Software: LTspice, PSpice (OrCAD), Cadence (schematic and simulation), OrCAD PCB Editor, Logger Pro
Communication: technical reports, laboratory reports, data analysis summary, presentations (small audiences)
Languages: Korean (native), English (fluent)